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FACSIMILE COVER SHEET

TO: Examiner Melvin C. Mayes - United States Patent and Trademark Office; Art Unit - 1734

CLIENT NAME/NUMBER: WA390/64724

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FROM: Jack G. Abid **DATE:** February 16, 2007

NUMBER OF PAGES (INCLUDING COVER SHEET): 16

COMMENTS/INSTRUCTIONS:

Please see the attached Appeal Brief for U.S. Patent Application Serial No. 10/522,049.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: BYUN ET AL.	Examiner: M. MAYES
Serial No. 10/522,049	Art Unit: 2841
Filing Date: JANUARY 20, 2005	Attorney Docket No. 64724
For: METHOD FOR CONNECTING MICRO-CIRCUITS AND CONNECTION STRUCTURE BY THE SAME	

APPELLANT'S APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief together with the requisite $500.00 large entity fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. 01-0484.

(1) Real Party in Interest

The real party in interest is LG CABLE LTD., assignee of the present application as recorded at reel 016720, frame 0257.

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In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

(3) Status of the Claims

Claims 1-7 are pending in the application and stand rejected, all of which being appealed herein. Claims 8-17 have been canceled.

(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

Independent Claim 1, for example, is directed to a method for connecting microcircuits **11, 15**. The method comprises providing an insulating resin solution **16**, applying the insulating resin solution to each circuit board having circuit patterns **12-P, 14-P**, and aligning the circuit boards to face each other so that electrodes **12, 14** of the circuit boards face each other to connect the corresponding electrodes of the circuit patterns formed in each circuit board.

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

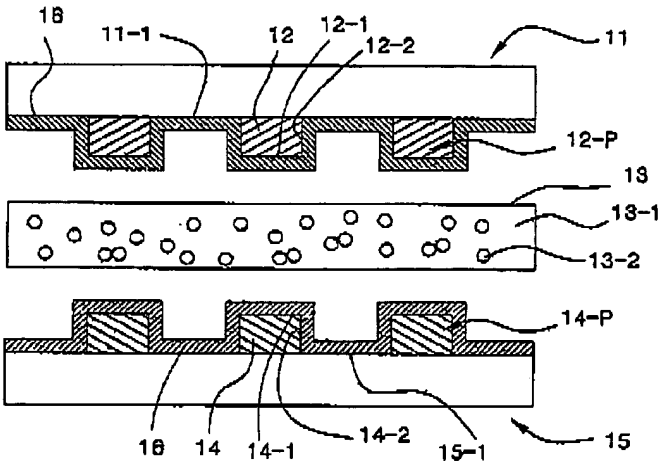

Figure 3 of the Present Application

The method further comprises positioning an anisotropic conductive adhesive **13** between the circuit boards **11, 15**, heating the circuit boards, and applying a predetermined pressure to a side of each circuit board opposite the anisotropic conductive adhesive so that corresponding electrodes **12, 14** are connected to each other. For applying the insulating resin solution **16**, the insulating resin solution is formed on a plain portion **12-1, 14-1** and a side portion **12-2, 14-2** of the circuit patterns and a bottom portion **11-1, 15-1** of the circuit board **11, 15**. (Figure 3, reproduced above, and the Specification of Present Application page 7, line 20 through page 12, line 4).

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**
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(6) Grounds of Rejection to be Reviewed On Appeal

The Examiner rejected Claims 1 and 5-7 over U.S. Patent No. 5,800,650 to Anderson et al. in view of U.S. Patent Application Publication No. 2003/0064147 to Fuji et al.

The Examiner rejected Claims 2-4 over the Anderson et al. patent in view of the Fuji et al. application and Japanese Patent Publication No. 2002-179761.

(7) Argument

The Examiner rejected independent Claim 1 over the Anderson et al. patent in view of the Fuji et al. patent application. The Anderson et al. patent discloses a laminating process for interconnecting laminates including respective opposing conductive layers and dielectric coverlayers. The Anderson et al. patent further discloses a conductive adhesive layer of non-conductive material with conductive particles to interconnect the laminates. (Col. 13, lines 6-26). The dielectric coverlayers are selectively screen-printed over the conductive layers. (Col. 13, lines 27-31). The Anderson et al. patent further discloses curing the dielectric ink within an oven. (Col. 13, lines 50-57). The Examiner correctly notes that the Anderson et al. patent does not disclose an insulating resin solution, as recited in independent Claim 1, and looks to the Fuji et al. application for such.

The Fuji et al. application discloses a method for applying resin solution to the surface of a printed circuit.

(Paragraphs 25-27). The Fuji et al. application further discloses subsequent drying of the resin to provide a hardened, electrically insulating, and impact resistant coverlayer. (Paragraph 29). The Fuji et al. application discloses a dryer exposing the resin to heat. (Paragraph 27; Claim 9). The Examiner contends it would have been obvious to use this method on the dielectric ink coverlayers disclosed in the Anderson et al. patent. The Examiner also contends that the motivation to combine the Anderson et al. patent and the Fuji et al. application is to provide a coverlayer with no voids.

Applicants respectfully submit that the Examiner's proposed combination of the Anderson et al. patent and the Fuji et al. application is improper because the proposed combination renders Anderson et al. unsatisfactory for its intended purpose. Indeed, the Anderson et al. patent teaches that the dielectric coverlayers are preferably selectively screen-printed over the conductive layers with a number of openings and apertures. (Col. 13, lines 26-31). In the alternative, the dielectric ink can be applied across the entire surface with subsequent laser or chemical etching to create the needed openings in the dielectric layer. (Col. 13, lines 32-45). Further, Applicants submit that the properties of the dielectric ink are critical to the operation of Anderson et al. Applicants point out that the Anderson et al. patent teaches that the metal-film laminate, (Col. 7, line 42), and the conductive adhesive, (Col. 15, line 65), may alternatively be in the form of a resin. Yet, the

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

Anderson et al. patent discloses no such capability for the dielectric ink. For this reason alone, there is no proper motivation to combine disjoint pieces of the prior art as the Examiner contends.

Moreover, Applicants submit that the proposed combination of the Anderson et al. patent and the Fuji et al. application is improper also because the proposed combination changes the principle of operation of Anderson et al. More specifically, Applicants submit that the proposed combination produces a result that is inoperable. As recited in independent Claim 1, the claimed method includes heating the circuit boards and subsequently applying a predetermined pressure to a side of each circuit board opposite the anisotropic conductive adhesive so that corresponding electrodes are connected to each other.

As suggested by the Examiner, if the resin of Fuji et al. was used to modify the Anderson et al. patent, the result would be inoperable since the heat-cured resin of Fuji et al. would have been heated prior to the joining step. Using the now hardened, impact resistant, and electrically insulating resin of the Fuji et al. application, the conductive particles of the Anderson et al. patent would not penetrate the resin, in contrast to the embedded conductive particles depicted in Figure 2 of the Anderson et al. patent. Accordingly, for this reason also, there is no proper motivation to combine the references in the manner suggested by the Examiner.

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

In response to the Applicant's argument, the Examiner contends that the Fuji et al. application is cited in the proposed combination simply to provide the process of applying the coverlayer from a resin solution and not the particular resin taught by the reference. Applicants submit that one of ordinary skill in the art, when considering combining the dielectric ink coverlayer of the Anderson et al. patent with the insulating coverlayer of the Fuji et al. application, would be taught away from the combination due to the aforementioned characteristics of the resin. A person of ordinary skill in the art will not selectively seize on the resin property of the Fuji et al. application while ignoring the fact that the actual resin taught would produce an inoperative result.

The Examiner also contends that the Fuji et al. application's resin solution process does not require heat-based drying. Thereby, the result of the proposed combination would be operable. Although, Applicants disagree with this contention by the Examiner and point to paragraph 27 and Claim 9 of the Fuji et al. application, Applicants note that the Examiner's proposed combination is an attempt to produce the claimed invention, and the claimed invention requires "heating the circuit boards", as recited in Claim 1.

Accordingly, it is submitted that independent Claim 1 is patentable over the prior art. Its respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

discussion herein. Applicants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner and withdraw the current rejection of the claims.

In re Patent Application of:
BYUN, II ET AL.
Serial No. 10/522,049
Filing Date: **JANUARY 20, 2005**

CONCLUSIONS

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable decision by the Examiner.

Respectfully submitted,

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CERTIFICATE OF FACSIMILE TRANSMISSION

I HEREBY CERTIFY that the foregoing correspondence has been forwarded via facsimile number 571-273-8300 to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 this 16th day of February, 2007.

Dawn K. Kim

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

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APPENDIX A - CLAIMS ON APPEAL
FOR U.S. PATENT APPLICATION SERIAL NO. 10/522,049

1. A method for connecting microcircuits comprising:

(a) providing an insulating resin solution;

(b) applying the insulating resin solution to each circuit board having circuit patterns;

(c) aligning the circuit boards to face each other so that electrodes of the circuit boards face each other, in order to connect the corresponding electrodes of the circuit patterns formed in each circuit board;

(d) positioning an anisotropic conductive adhesive between the circuit boards;

(e) heating the circuit boards; and

(f) applying a predetermined pressure to a side of each circuit board opposite the anisotropic conductive adhesive so that corresponding electrodes are connected to each other;

wherein in the (b) step, said insulating resin solution is formed on a plain portion and a side portion of the circuit patterns and a bottom portion of the circuit board.

2. The method of claim 1, wherein in the (a) step said insulating resin solution is prepared by dissolving a thermoplastic resin having a softening point in the range of 60 to 150°C or a compound of the thermoplastic resin into a solvent.

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

3. The method of claim 2, wherein the thermoplastic resin is selected from the group of consisting of polyethylene resin, ethylene copolymer resin, ethylene vinyl acetate copolymer resin, ethylene-acrylic acid copolymer resin, ethylene acrylic acid ester copolymer resin, poly amide resin, poly ester resin, styrene butadiene copolymer resin, ethylene-propylene copolymer resin, acrylic acid ester rubber, acrylonitrile-butadiene copolymer resin, phenoxy resin, thermoplastic epoxy resin, poly urethane resin, poly vinyl acetal resin and poly vinyl butilal resin.

4. The method of claim 1, wherein in the (a) step said insulating resin solution is prepared by dissolving thermoplastic resin having a softening point in the range of 80 to 120°C or a compound of the thermoplastic resin into a soluble solvent.

5. The method of claim 1, wherein in the (b) step said insulating resin solution produces a film layer having a thickness of 0.1 to 5μm on the circuit board.

6. The method of claim 1, wherein in the (b) step said insulating resin solution produces a film layer having a thickness of 0.3 to 3μm on the circuit board.

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

7. The method of claim 1, wherein the anisotropic conductive adhesive includes an insulating component, and conductive particles dispersed in the insulating component.

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

APPENDIX B – EVIDENCE APPENDIX PURSUANT TO 37 C.F.R. § 41.37(c)(1)(ix)

None.

In re Patent Application of:
BYUN, II ET AL.
Serial No. **10/522,049**
Filing Date: **JANUARY 20, 2005**

APPENDIX C - RELATED PROCEEDINGS APPENDIX
PURSUANT TO 37 C.F.R. § 41.37(c)(1)(x)

None.